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ONS00393
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Date:	5/27/2005
IN RE APPLICATION OF:	Evgueniy Nikolov Stefanov
APPLN. NO.:	10/615171
FILED:	7/9/2003
FOR:	SYMMETRICAL HIGH FREQUENCY SCR STRUCTURE AND METHOD
Group:	2815
Examiner:	Matthew E. Warren 571-272-1737

CERTIFICATE OF TRANSMITTAL VIA FACSIMILE

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO THE PATENT AND TRADEMARK OFFICE, ATTN EXAMINER Matthew E. Warren AT THE FAX No. (703) 872-9306

By

Lydia McNamara _____ on: May 27, 2005
Lydia McNamara Date

NUMBER OF PAGES INCLUDING THIS COVER PAGE: 20

Fee Sheet (1)
Briefs (13)
Amendment (6)

Inc

PTO/SB/17 (10-03)
Approved for use through 07/31/2006 OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Appliation Number	10/615171
Filing Date	July 9, 2003
First Named Inventor	Evgueniy N. Stefanov et al
Examiner Name	Matthew E. Warren
Art Unit	2815
Attorney Docket No.	ONS00393

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account.

Deposit Account Number: 501086

Deposit Account Name: Semiconductor Components Industries, L.L.C.

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X	=
Independent Claims		- 3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) 1811 1 20(1) Certificate of Correction

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 500.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Kevin B. Jackson	*Registration No. (Attorney/Agent)*	38,502	*Telephone*	(602) 244-4885
Signature				*Date*	5/27/2005

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ONS00393
10/615,171

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	RESPONSE UNDER 37 CFR 1.116
	:	EXPEDITED PROCEDURE
Evgueniy N. Stefanov et al.	:	EXAMINING GROUP 2815
	:	
Serial No.: 10/615,171	:	
Filed: July 9, 2003	:	Examiner: Matthew E. Warren

For: **SYMMETRICAL HIGH FREQUENCY SCR STRUCTURE**

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, attn: **Examiner Matthew Warren**

FAX No. (703) 872-9306 on May 27, 2005

By Signature: Lydia McNamara

Lydia McNamara (602.244.5306)

APPEAL BRIEF

I. REAL PARTY OF INTEREST

The real party of interest in this appeal is Semiconductor Components Industries, LLC (SCI), doing business as ON Semiconductor.

II. RELATED APPEALS AND INTERFERENCES

Applicants are not aware of any related appeals or interferences to this application.

III. STATUS OF THE CLAIMS

Claims 1-20 are in the proceeding. Claims 1-8 are the claims on appeal. A copy of the claims on appeal is provided in Section VIII., Claims Appendix.

Claims 1-8 are rejected.
Claims 9-15 are cancelled.
Claims 16-20 are withdrawn in view of a restriction requirement.

IV. STATUS OF THE AMENDMENTS

An Election was filed on May 3, 2004 and entered into the record. An amendment was filed on October 12, 2004 and entered into the record. A Response to the Final Rejection was filed on March 2, 2005 but was not entered into the record. An Amendment After Final canceling claims 9, 11, 12, 13, 14, and 15 is filed concurrently with this Appeal Brief as allowed pursuant to § 41.33 (b).

V. SUMMARY OF CLAIMED SUBJECT MATTER

The structure of claim 1 calls for a high frequency integrated circuit structure, as described on page 7, line 12 through page 10, line 35, and shown in FIG. 5, comprising a body of semiconductor material (417) having a plurality of isolated

active regions (see more specifically p. 9, l. 4-9). The body semiconductor material (417) has a first conductivity type. Internal circuitry (53) is formed in a first active region. As described more specifically on page 7, lines 20-29, a second active region comprising a buried layer (413) of a second conductivity type is formed over the body of semiconductor material (417) and a first semiconductor layer (414) of the second conductivity type is formed over the buried layer (413). The first semiconductor layer (414) has a lower dopant concentration than the buried layer (413).

How the layers and regions comprising the first and second controller rectifier devices are formed is described on page 8, line 1 through page 9, line 36. As stated in claim 1, a first silicon controlled rectifier (p-n-p-n) device is formed in the second active region. The first silicon controlled rectifier device comprises: a first well region (411) of the first conductivity type formed in the first semiconductor layer 414 and a first doped region (415) of the first conductivity type formed in the first well region (411); the buried layer (413); a second well region (421) of the first conductivity type formed in the first semiconductor layer (414) and spaced apart from the first well region (411); and a second doped region (422) of the second conductivity type formed in the second well region (421). As stated on page 11, lines 4-12, the first silicon controlled device is a p-n-p-n device formed by layers or regions (415 and 411)*p* - (413)*n* - (421)*p* - (422)*n*.

As further described on page 11, lines 4-12, a second silicon controlled rectifier (p-n-p-n) device comprises: the second well region (421) and a third doped region (425) of the first conductivity type formed in the second well region (421); the buried layer (413); the first well region (411); and a fourth doped region (412) of the second conductivity type formed in the first well region (411). As stated on page 11, lines 4-12, the

second silicon controlled device is a p-n-p-n device formed by layers or regions p (425 and 421)*p* - (413)*n* - (411)*p* - (412)*n*.

As shown in Fig. 9, the first and second silicon controlled rectifier devices are coupled to the internal circuitry (53) and form an ESD structure for protecting the internal circuitry (53) against positive and negative ESD stresses.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Rejection of claims 1-4, 6, and 7 under 35 U.S.C. §103 as being obvious over Wang et al., USP 6,365,924 (hereinafter "Wang") in view of Mori, USP 4,246,594 (hereinafter "Mori").

B. Rejection of claims 5 under 35 U.S.C. §103 as being obvious over Wang in view of Mori, and further in view of Duvvury et al., USP 6,365,940 (hereinafter "Duvvury").

C. Rejection of claim 8 under 35 U.S.C. §103 as being obvious over Wang in view of Mori, and in further view of Pavier et al., US Pub 2003/0062622 (hereinafter "Pavier").

VII. ARGUMENT

A. Arguments for allowability of Claims 1-4, 6, and 7 over Wang in view of Mori.

1. Claims 1-3, 5, and 7.

Applicants respectfully submit that Wang in view of Mori fails to make claim 1 obvious for the following reasons.

Applicants respectfully assert that there is no motivation to combine the two references. It is well accepted that obviousness can only be established by combining the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Specifically, the Wang reference teaches a CMOS implementation

(see column 4, line 31) of a dual direction SCR device, while the Mori reference teaches a conventional bipolar implementation of a stand alone unidirectional SCR switch. Moreover, Wang does not suggest that his device is suitable for a bipolar implementation, and Mori does not suggest that his device is suitable for a CMOS implementation.

Additionally, Mori's SCR structure is not symmetrical and thus is not conducive to forming an ESD structure for protecting internal circuitry against positive and negative ESD stresses. Specifically, Mori's structure places an individual SCR in each cell, and these SCR's comprise individual and isolated PNPN devices (regions 14, 18, 20, and 22), which are not symmetrical as evident in FIG. 3a.

In response to the Examiner's statement that there is sufficient motivation to combine because "both references still teach SCR devices" is not convincing because it ignores the key differences between the references set forth above. Obvious to try is not an accepted standard.

Absent applicants' invention as a roadmap to motivate the combination, applicants respectfully submit that there is no motivation to combine the references, and the obviousness rejection should be withdrawn.

Assuming, arguendo, that there is motivation to combine the two references, the combination of Wang and Mori still does not make claim 1 obvious for several reasons. Specifically, claim 1 calls for the first and second well regions to be of one conductivity type, and the buried layer to be of a second conductivity type. In Mori, his buried layer is the same conductivity type as his well region 14.

Additionally, since Mori's device is unidirectional, he uses individual or separate buried layers for each device, and there is no suggestion of one buried layer being part of two devices as called for in claim 1. Applicant's first and second silicon controlled rectifier is comprised of the buried layer (413) (see

claim 1, "the buried layer" recited in line 10 and line 16 of claim 1). In fact, it is clear from Mori's FIG. 3a that his individual devices are separated by a large resistance R_8.

Furthermore, the teaching of Mori would suggest at best placing a buried layer below Wang's diffused N-Well 116, and thus, it would not even be part of the two SCR devices as called for in claim 1. It would simply lower resistance as taught in the Mori reference. Applicants further submit that this is not a minor difference because with their implementation with the buried layer being part of the SCR devices, the buried layer provides, among other things, a relatively high holding voltage, which allows applicants' structure to overcome deficiencies of prior art structure like Wang's, which have a tendency to remain in a clamped "on" state when parasitic triggering events occur (see paragraphs [0027] and [0040] in applicants' specification).

It is further accepted that a prima facie case of obviousness cannot be properly made if a proposed modification or combination would destroy or impair the function of the device disclosed in a reference. The combination of Wang and Mori would destroy or impair the intended function of the Wang device. In re Gordon, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). Since Wang's structure is specifically shown as a CMOS implementation, isolation in conventional CMOS technology is achieved by the fact that the junction formed between the P-substrate and the N-Well 116 is under a reverse bias high enough to isolate Wang's SCR. By adding a higher doped buried layer to Wang's structure, the reverse breakdown voltage between the P-substrate and N-Well 116 would be significantly lowered thereby destroying or impairing the isolation of the SCR device and thus, destroying or impairing functionality of Wang's device.

For the reasons set forth above, applicants respectfully submit that the combination of Wang and Mori fails to make claim 1 obvious.

Claims 2 and 3 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claims 6 and 7 depend from claim 2 and are believed allowable for at least the same reasons as claim 2.

2. Claim 4.

Claim 4 depends from claim 2 and further calls for "a deep contact trench extending from the first surface of the first semiconductor layer into the semiconductor wafer." Claim 4 is believed allowable for the same reasons as claims 1 and 2. Additionally, claim 4 is believed allowable because neither reference teaches a trench contact. In Mori, diffused regions are taught. Moreover, Mori's diffused regions do not extend to his substrate 24 as called for in claim 4.

B. Arguments for allowability of claim 5 over Wang in view of Mori and Duvvury.

Claim 5 was rejected under 35 U.S.C. §103 as being obvious over Wang in view of Mori, and further in view of Duvvury et al. Applicants respectfully submit that the Duvvury reference does not make up the deficiencies of Wang and Mori, as discussed above.

Claim 5 depends from claim 1 and thus, is believed allowable for at least the same reasons as claim 1.

C. Arguments for allowability of claim 8 over Wang in view of Mori and Pavier.

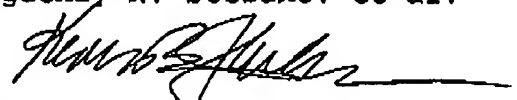
Claim 8 was rejected under 35 U.S.C. §103 as being obvious over Wang in view of Mori, and in further view of Pavier et al. Applicants respectfully submit that the Pavier reference does not make up for the deficiencies of Wang and Mori as discussed above.

Claim 8 depends from claim 1 and further calls for "a deep isolation trench formed in the body of semiconductor material for isolating the ESD structure from the internal circuitry, wherein

the deep isolation trench includes a dielectric layer." Applicants respectfully submit that claim 8 is allowable for the same reasons as claim 1. Additionally, applicants respectfully submit that absent applicants' invention as a roadmap, there is simply no motivation whatsoever to combine the Pavier reference with Wang and Mori. Specifically, Pavier is not dealing with ESD issues, nor he is dealing with SCR devices. Thus, applicants submit that claim 8 is allowable for this additional reason.

In view of the above, it is believed that the claims are allowable, and the Board of Appeals and Interferences is respectfully requested to reverse the Examiner.

Respectfully submitted,
Evgueniy N. Stefanov et al.



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Date: May 27, 2005

VIII. CLAIMS APPENDIX

1. (amended): A high frequency integrated circuit structure comprising:

a body of semiconductor material having a plurality of isolated active regions, and comprising a first conductivity type;

internal circuitry formed in a first active region;

a second active region comprising a buried layer of a second conductivity type formed over the body of semiconductor material and a first semiconductor layer of the second conductivity type formed over the buried layer, wherein the first semiconductor layer has a lower dopant concentration than the buried layer;

a first silicon controlled rectifier device formed in the second active region, the first silicon controlled rectifier device comprising a first well region of the first conductivity type formed in the first semiconductor layer, a first doped region of the first conductivity type formed in the first well region, the buried layer, a second well region of the first conductivity type formed in the first semiconductor layer and spaced apart from the first well region, and a second doped region of the second conductivity type formed in the second well region; and

a second silicon controlled rectifier device comprising the second well region, a third doped region of the first conductivity type formed in the second well region, the buried layer, the first well region, and a fourth doped region of the second conductivity type formed in the first well region, wherein the first and second silicon controlled rectifier devices are coupled to the internal circuitry and form an ESD structure for protecting the internal circuitry against positive and negative ESD stresses.

2. (amended): The high frequency integrated circuit structure of claim 1 wherein the body of semiconductor material comprises:

a semiconductor wafer having the first conductivity type; and

a second semiconductor layer formed over the semiconductor wafer, wherein the second semiconductor layer comprises the first conductivity type, and wherein the second semiconductor layer has a lower dopant concentration than the semiconductor wafer, and wherein the buried layer is formed adjacent the second semiconductor layer.

3. (original): The high frequency integrated circuit device of claim 2 further comprising:

a first ohmic contact coupling the first and fourth doped regions; and

a second ohmic contact coupling the second and third doped regions.

4. (amended): The high frequency integrated circuit device of claim 2 further comprising a deep contact trench extending from a surface of the first semiconductor layer into the semiconductor wafer.

5. (amended): The high frequency integrated circuit device of claim 1 further comprising a field dielectric region formed on a surface of the first semiconductor layer between the first and second wells.

6. (amended): The high frequency integrated circuit structure of claim 2, wherein the second semiconductor layer has a dopant concentration of approximately $1.0x10^{13}$ atoms/cm^3

7. (amended): The high frequency integrated circuit structure of claim 2, wherein the second semiconductor layer has a thickness from about 1.5 microns to about 3.0 microns.

8. (amended): The high frequency integrated circuit structure of claim 1 further comprising a deep isolation trench formed in the body of semiconductor material for isolating the ESD structure from the internal circuitry, wherein the deep isolation trench includes a dielectric layer.

Claim 9 (cancelled).
Claim 10 (cancelled).
Claim 11 (cancelled).
Claim 12 (cancelled).
Claim 13 (cancelled).
Claim 14 (cancelled).
Claim 15 (cancelled).

16. (withdrawn): A method for forming a high frequency SCR device including the steps of:

providing a semiconductor substrate including a first semiconductor layer of a first conductivity type, a second semiconductor layer of a second conductivity type over the first semiconductor layer, and a third semiconductor layer over the second semiconductor layer, wherein the third semiconductor layer comprises the second conductivity type, and wherein the third semiconductor layer has a lower dopant concentration than the second semiconductor layer;

forming first and second wells in the third semiconductor layer, wherein the first and second wells comprise the first conductivity type, and wherein the first and second wells are spaced apart;

forming first and second doped regions in the first well, wherein the first doped region comprises the first conductivity

type, and the second doped region comprises the second conductivity type; and

forming third and fourth doped regions in the second well, wherein the third doped region comprises the first conductivity type, and wherein the fourth doped region comprises the second conductivity type.

17. (withdrawn): The method of claim 16 wherein the step of providing the semiconductor substrate includes providing a semiconductor substrate having a fourth semiconductor layer formed between the first semiconductor layer and the second semiconductor layer, wherein the fourth semiconductor layer comprises the first conductivity type, and wherein the fourth semiconductor layer has a lower dopant concentration than the first semiconductor layer.

18. (withdrawn): The method of claim 16 further comprising the steps of:

forming an isolation region on a surface of the third semiconductor region between the first and second wells;

forming a first ohmic contact coupling the first and second doped regions; and

forming a second ohmic contact coupling the third and fourth doped regions.

19. (withdrawn): The method of claim 16 further comprising the step of forming a deep isolation trench that surrounds the high frequency SCR device, and that extends from a surface of the third semiconductor layer into the first semiconductor layer.

20. (withdrawn): The method of claim 16 further comprising the step of forming a deep contact trench extending from a surface of the third semiconductor layer into the first semiconductor layer.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to § 1.130, 1.131, 1.132.

X. RELATED PROCEEDINGS APPENDIX

The appellant is not aware of any related proceedings.